M.E. (Embedded Systems)

2015 Regulations, Curriculum & Syllabi

BANNARI AMMAN INSTITUTE OF TECHNOLOGY

(An Autonomous Institution Affiliated to Anna University, Chennai
Approved by AICTE - Accredited by NBA New Delhi, NAAC with 'A' Grade and ISO 9001:2008 Certified)
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PROGRAM EDUCATIONAL OBJECTIVES (PEOs)

I. The Graduates of Embedded Systems will demonstrate their skills to meet the current and future industrial challenges in the field of embedded systems engineering.

II. The Graduates of Embedded Systems will exhibit their skills to take-up hardware/software co-design for embedded systems.

III. The Graduates of Embedded Systems will undertake a significant research or development projects.

PROGRAM OUTCOMES (POs)

(a) able to apply knowledge from undergraduate engineering and other disciplines to identify, formulate, solve novel advanced electronics engineering along with soft computing problems that require advanced knowledge within the field

(b) able to understand and integrate new knowledge within the field.

(c) able to apply advanced technical knowledge in multiple contexts

(d) able to understand and design advanced electronics systems (Analog and Digital Systems) and conduct experiments, analyze and interpret data.

(e) able to design, execution and evaluation of experiments on embedded platforms.

(f) able to analysis, design and testing of systems that include both hardware and software.

(g) able to convey technical material through formal written reports which satisfy accepted standards of writing style.

(h) able to Demonstrate effective communication skills in oral, written and electronic media.

(i) able to become knowledgeable about contemporary developments.

(j) Continue to improve their professional value through lifelong learning.

MAPPING OF PEOs AND POs

PEO(s)	Programme Outcome (s)										
	(a)	(b)	(c)	(d)	(e)	(f)	(g)	(h)	(i)	(j)	(k)
I	x	x	x								
II	x	x	x	x	x	x		x		x	
III	x			x	x		x		x		x

M.E. Embedded Systems

Minimum credits to be earned: 76

First Semester							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
15ES11	Discrete Mathematics and Automata Theory[δ]	I,III,IV	(a), (c), (d), (e), (f)	3	2	0	4
15ES12	Embedded Linux	I,II,IV	(a), (b), (d), (e),(f)	3	2	0	4
15ES13	Digital System Design	I,IV,V	(a),(c),(d),(e)	3	2	0	4
15ES14	Embedded Computing System Design	I,II,V	(a), (b), (e), (f)	3	0	0	3
15ES15	ARM Processors and Controllers	I,II,IV	(a), (b), (c), (d)	3	0	0	3
	Elective - I			3	0	0	3
15ES17	Processors and Controllers Laboratory	I,II,III	(a), (b), (c), (d), (e)	0	0	2	1
15ES18	Embedded Operating Systems Laboratory	II,III,IV	(a), (b), (c), (d), (e), (f)	0	0	2	1
15GE19	Business English - I[α]			1	0	2	2
			Total	**19**	**6**	**6**	**25**
Second Semester							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
15ES21	Research Methodology			3	0	0	3
15ES22	Real Time Operating Systems	I,II,IV	(g), (h), (k), (l)	3	2	0	4
15ES23	Embedded Systems Architecture	I,II,IV	(a), (b), (c), (d)	3	2	0	4
15ES24	Soft Computing Techniques	II,III,IV	(a),(c),(e),(f)	3	2	0	4
	Elective II			3	0	0	3
	Elective III			3	0	0	3
15ES27	Real Time Operating Systems Laboratory	I,II,IV	(a), (b), (c),(d), (e),(f)	0	0	2	1
15ES28	Technical Seminar	II,III,IV	(a), (c), (d), (e), (f), (g), (h),(i)	0	0	2	1
15GE29	Business English - II[α]			1	0	0	1
			Total	**19**	**6**	**4**	**24**
Third Semester							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
	Elective IV			3	0	0	3
	Elective V			3	0	0	3
	Elective VI			3	0	0	3
15ES34	Project Work - Phase I and Viva Voice	II,III,V	(a), (c), (d), (e), (f), (g), (h)	-			6
			Total	**9**	**0**	**0**	**15**
Fourth Semester							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
15ES41	Project Work - Phase II and Viva Voice	II,III,V	(a), (c), (d), (e), (f), (g), (h)	-			**12**

[δ] Common to Embedded Systems and Computer Science & Engineering

[α] Common to all M.E. / M.Tech. Programmes

ME Embedded Systems (Part Time)

Code No.	Course	Objectives & Outcomes		L	T	P	C
		PEOs	POs				
First Semester							
15ES11	Discrete Mathematics and Automata Theory[δ]	I,III,IV	(a), (c), (d), (e), (f)	3	2	0	4
15ES12	Embedded Linux	I,II,IV	(a), (b), (d), (e),(f)	3	2	0	4
15ES13	Digital System Design	I,IV,V	(a),(c),(d),(e)	3	2	0	4
15ES17	Processors and Controllers Laboratory	I,II,III	(a), (b), (c), (d), (e)	0	0	2	1
15GE19	Business English - I[α]			1	0	2	2
			Total	**10**	**6**	**4**	**15**
Second Semester							
15ES21	Research Methodology			3	0	0	3
15ES22	Real Time Operating Systems	I,II,IV	(g), (h), (k), (l)	3	2	0	4
15ES23	Embedded Systems Architecture	I,II,IV	(a), (b), (c), (d)	3	2	0	4
15ES27	Real Time Operating Systems Laboratory	I,II,IV	(a), (b), (c),(d), (e),(f)	0	0	2	1
15GE29	Business English - II[α]			1	0	0	1
			Total	**10**	**4**	**2**	**13**
Third Semester							
15ES14	Embedded Computing System Design	I,II,V	(a),(b),(e),(f)	3	0	0	3
15ES15	ARM Processors and Controllers	I,II,IV	(a), (b), (c), (d)	3	0	0	3
15ES24	Soft Computing Techniques	II,III,IV	(a),(c),(e),(f)	3	2	0	4
15ES18	Embedded Operating Systems Laboratory	II,III,IV	(a),(b),(c),(d), (e), (f)	0	0	2	1
			Total	**9**	**2**	**2**	**11**
Fourth Semester							
	Elective I			3	0	0	3
	Elective II			3	0	0	3
	Elective III			3	0	0	3
15ES28	Technical Seminar	II,III,IV	(a),(c),(d),(e),(f),(g), (h),(i)	0	0	2	1
			Total	**9**	**0**	**2**	**10**
Fifth Semester							
	Elective IV			3	0	0	3
	Elective V			3	0	0	3
	Elective VI			3	0	0	3
15ES34	Project Work - Phase I	II,III,V	(a),(c),(d),(e),(f),(g),(h)	-	-	-	6
			Total	**9**	**0**	**0**	**15**
Sixth Semester							
15ES41	Project Work - Phase II	II,III,V	(a), (c), (d), (e), (f), (g), (h)	-			**12**

[δ] Common to Embedded Systems and Computer Science & Engineering

[α] Common to all M.E. / M.Tech. Programmes

List of Core Electives							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
15ES51	Multiprocessor	I,II,IV	(a), (b), (d)	3	0	0	3
15ES52	Statistical Signal Processing[$]	I,II,IV	(a),(b), (c), (e), (f)	3	0	0	3
15ES53	Embedded Networking[Δ]	I,II,IV	(a), (c), (e), (f)	3	0	0	3
15ES54	Software for Embedded Systems	I,III,IV	(a), (c), (d), (f)	3	0	0	3
15ES55	Industrial Robotics	III,IV,V	(a), (b), (d), (e)	3	0	0	3
15ES56	Automotive Networking	III,IV,V	(a), (b), (d), (f)	3	0	0	3
15ES57	Image Processing Techniques	I,IV	(a), (b), (c), (e)	3	0	0	3
15ES58	Hardware Description Language	I,III	(a),(b),(e),(h),(j)	3	0	0	3
15ES59	Information Theory and Coding	I,II,IV	(a), (b), (c), (d)	3	0	0	3
15ES60	System on Chip[Δ]	I,II,IV	(a),(b), (c), (e), (f)	3	0	0	3
15ES61	Low Power VLSI Design	II,IV,V	(a), (b), (c), (f), (h)	3	0	0	3
15ES62	Pattern Recognition and Artificial Intelligent Techniques[ϒ]	I,II,III	(a), (b), (e), (f)	3	0	0	3
15ES63	Design of Embedded Control Systems	I,III,IV	(a), (b), (e), (f)	3	0	0	3
15ES64	Graphical System Design	I,III,V	(a), (b), (e), (f)	3	0	0	3
15ES65	ASIC Design[Δ]	I,II,IV	(a), (b), (c), (d), (e)	3	0	0	3
15ES66	Wireless and Mobile Communication	I,III,IV	(a), (d), (e), (f)	3	0	0	3
15ES67	Distributed Embedded Computing	I,II,IV	(a), (b), (c), (d)	3	0	0	3
15ES68	Fault Tolerance Computing	I,II,IV	(a), (b), (c), (e)	3	0	0	3
15ES69	Analog Interfacing	I,III,IV	(a), (b), (c), (f)	3	0	0	3
15ES70	Operating Systems	II,III,IV	(f),(c),(d),(e)	3	0	0	3
15ES71	Network On Chip[Δ]	I,II,IV	(a), (b), (c), (e), (g)	3	0	0	3
One Credit Courses							
Code No.	**Course**	**Objectives & Outcomes**		**L**	**T**	**P**	**C**
		PEOs	**POs**				
15ESXA	Quad Core	III, IV	(d), (e), (f)	1	0	0	1
15ESXB	Arduino	III,IV	(d), (e), (f)	1	0	0	1
15ESXC	ATMEL	III,IV	(d), (e), (f)	1	0	0	1

[$] Common to Applied Electronics, Embedded Systems and Communication Systems

[Δ] Common to Embedded systems and VLSI Design

[ϒ] Common to Embedded systems and Applied Electronics

15ES11/15CS11 DISCRETE MATHEMATICS AND AUTOMATA THEORY
(Common to Embedded Systems & Computer Science and Engineering)

3 2 0 4

Course Objectives

- To understand and use the terms cardinality, finite and countably infinite and determine which of these characteristics is associated with a given set.
- To construct simple mathematical proofs and posses the ability to verify them.
- To solve counting problems involving the multiplication rule, permutations and combinations.
- To present some of the often encountered discrete and automata theory models and their applications
- To introduce graphs as a powerful modeling tool that can be used to solve practical problems in various fields.

Course Outcomes (COS)

1. Check the validity of the arguments.
2. Understand how to construct correct mathematical arguments.
3. Check whether a particular combination of words is a valid sentence or not
4. To apply the abstract concepts of graph theory in modeling and solving non-trivial problems in different fields of study.

Unit I

Fundamental Structures

Set theory - Relationships between sets - Operations on sets - Set identities - Principle of inclusion and exclusion - Minsets. Relations: – Binary relations - Partial orderings - Equivalence relations. Functions: – Properties of functions - Composition of functions – Inverse functions - Permutation functions. **9 Hours**

Unit II

Logic

Propositional logic – Logical connectives – Truth tables – Normal forms (conjunctive and disjunctive) - Predicate logic - Universal and existential quantifiers - Proof techniques – Direct and indirect – Proof by contradiction – Mathematical Induction.

9 Hours

Unit III

Combinatorics

Basics of counting – Counting arguments – Pigeonhole principle - Permutations and Combinations - Recursion and Recurrence relations – Generating functions.

9 Hours

Unit IV

Modeling Computation and Languages

Finite state machines – Deterministic and Non- deterministic finite state machines –Equivalence of DFA and NFA - Formal Languages – Classes of Grammars – Type_0 – Context Sensitive – Context Free – Regular Grammars .

9 Hours

Unit V

Graph Theory

Introduction to Graphs- Graphs operations-Graph and Matrices-Graph Isomorphism- Connected Graphs- Euler Graphs- Hamilton paths and circuits-Shortest path problem.

9 Hours

Unit VI[$]

Algebraic laws for Regular Languages- Pumping Lemma and Applications- Properties of Regular Languages- Parse trees and Language Pushdown Automaton.

Total: 45 +30 Hours

Reference(s)

1. Kenneth H. Rosen, *Discrete Mathematics and its Applications*, Tata McGraw Hill Publications, New Delhi. 7th Edition, 2011.
2. Trembly J.P. and Manohar R., *Discrete Mathematical Structures with Applications to Computer Science*, Tata McGraw Hill Publications Co. Ltd., New Delhi 2008..
3. Alan Doerr and Kenneth Levasseur, *Applied Discrete Structures for Computer Science*, Galgotia Publications Pvt. Ltd. Delhi. 2010.
4. Ralph P Girmaldi and B.V. Ramana, *Discrete and Combinatorial Mathematics: An Applied Introduction*, Fifth Edition, Pearson Education Asia, Delhi, 2007.
5. J.E. Hopcroft, R. Motwani and J.D. Ullman, Introduction *to Automata Theory, Languages and Computations*, Second Edition, Pearson Education, 2003.

15ES12 EMBEDDED LINUX

3 2 0 4

Course Objective

- To study the fundamentals of operating systems.
- To understand Linux operating measurement systems.
- To obtain basic knowledge on board support packages and device drivers.

Course Outcomes (COs)

The student will be able to

1. Apply and integrate theory and practical which has been studied to solve the engineering problems.
2. Develop the suitable research methodology for the project.
3. Present and justify/defend the project proposal.

Unit I

Fundamentals of Operating Systems

Overview of operating systems, Process and threads, Processes and Programs, Programmer view of processes, OS View of processes, Threads, Scheduling, Non preemptive and preemptive scheduling, Real Time Scheduling, Process Synchronization, Semaphores, Message Passing, Mailboxes, Deadlocks, Synchronization and scheduling in multiprocessor Operating Systems.

9 Hours

Unit II

Linux Fundamentals

Introduction to Linux, Basic Linux commands and concepts, Logging in, Shells, Basic text editing, advanced shells and shell scripting, Linux File System, Linux programming, Processes and threads in Linux, Inter process communication, Devices, Linux System calls.

9 Hours

Unit III

Embedded Linux

Embedded Linux-Introduction, Advantage, Embedded Linux Distributions, Architecture, Linux kernel architecture, User space, Linux startup sequence, GNU cross platform Tool chain.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit IV

Board Support Package and Embedded Storage

Inclusion of BSP in kernel build procedure, Boot loader Interface, Memory Map, Interrupt Management, PCI Subsystem, Timers, UART, Power Management, Embedded Storage, Flash Map, Memory Technology Device (MTD) –MTD Architecture, MTD Driver for NOR Flash.

9 Hours

Unit V

Embedded Drivers and Application Porting

Linux serial driver, Ethernet driver, I2C subsystem, USB gadgets, Watchdog timer, Kernel Modules, Application porting roadmap, Programming with threads, Operating System Porting Layer, Kernel API Driver, Case studies - RT Linux – uClinux.

9 Hours

Unit VI[$]

Embedded Storage: The Flash Mapping drivers, MTD Block and character devices, mtdutils package, Embedded File Systems, Optimizing storage space – Turning kernel memory.

Total: 45+30 Hours

Reference(s)

1. Paul Cobbaut, *Fundamental Linuxt* , Netsec BVBA, 2015.
2. P.Raghavan , *Embedded Linux System Design and Development*, Taylor & Francis, 2012.
3. Craig Hollabaugh , *Embedded Linux, Hardware, Software and Interfacing* , 2003.
4. Philippe Gerum, Karim Yaghmour , *Building Embedded Linux Systems*, 2009.
5. Christopher Hallinan , *Embedded Linux Primer: A Practical Real-World Approach*, 2nd ed, Prentice Hall, 2007.
6. www.linuxjournal.com.

15ES13 DIGITAL SYSTEM DESIGN

3 2 0 4

Course Objectives

- To understand the concepts of Asynchronous Sequential Circuit Design.
- To study the concepts of Fault Diagnosis and Testability Algorithms.
- To understand the concepts of System Design Using VHDL and Programmable Devices.

Course Outcomes (COs)

The student will be able to

1. Analyze and Design a sequential circuit.
2. Analyze and debug sequential circuits based on an abstract specification functionality.
3. Build a synchronous FPGA system in VHDL and verify its performance.

Unit I

Sequential Circuit Design

Analysis of Clocked Synchronous Sequential Networks (CSSN) Modeling of CSSN – State Stable Assignment and Reduction – Design of CSSN – Design of Iterative Circuits – ASM Chart–ASM Realization.

9 Hours

Unit II

Asynchronous Sequential Circuit Design

Analysis of Asynchronous Sequential Circuit (ASC) – Flow Table Reduction – Races in ASC– State Assignment–Problem and the Transition Table–Design of ASC – Static and Dynamic Hazards – Essential Hazards

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit III

Fault Diagnosis and Testability Algorithms

Fault Table Method – Path Sensitization Method – Boolean Difference Method – Kohavi Algorithm –Tolerance Techniques – The Compact Algorithm – Practical PLA's – Fault in PLA– Test Generation – Masking Cycle –DFT Schemes – Built –in Self Test.

9 Hours

Unit IV

Synchronous Design Using Programmable Devices

EPROM to Realize a Sequential Circuit – Programmable Logic Devices – Designing a Synchronous Sequential Circuit using a GAL – EPROM – Realization State machine using PLD– FPGA–Xilinx FPGA–Xilinx2000-Xilinx3000

9 Hours

Unit V

System Design Using VHDL

VHDL Description of Combinational Circuits – Arrays – VHDL Operators – Compilation and Simulation of VHDL Code–Modeling using VHDL – Flip Flops – Registers – Counters– Sequential Machine – Combinational Logic Circuits –

9 Hours

Unit VI[$]

VHDL Code for–Serial Adder, Binary Multiplier – Binary Divider–complete Sequential Systems – Design of a Simple Microprocessor.

Total: 45+30 Hours

Reference(s)

1. M. Morris Mano, Michael D.Ciletti, *"Digital System Design"*Pearson Education, 2008.
2. Charles H. Roth Jr., "*Digital System Design using VHDL"* Thomson Learning, 1998.
3. Charles H. Roth Jr., *Fundamentals of Logic design* Thomson Learning, 2004.
4. Donald G.Givone, *Digital principles and Design*, TataMcGrawHill, 2002.
5. John M.Yarbrough, *Digital Logic appns .and Design,*Thomson Learning, 2001.
6. Stephen Brown and Zvonk Vranesic, *Fundamentals of Digital Logic with VHDL Design*, TataMcGrawHill, 2002.
7. Mark Zwolinski, *Digital System Design with VHDL*PearsonEducation, 2004.

15ES14 EMBEDDED COMPUTING SYSTEM DESIGN

3 0 0 3

Course Objectives

- To study the overview of Embedded System Architecture
- To focus on distributed Embedded Architecture and its accessing protocols
- To understand about the design methodologies in hardware and software design

Course Outcomes (COs)

The student will be able to

1. Construct embedded system hardware.
2. Develop software programs to control embedded system.
3. Generate product specification for embedded system.

Unit I

Embedded Systems Overview

Embedded systems overview-design challenge-optimizing metrics - processor technology - IC technology - design technology-automation-synthesis-verification: hardware/software co - simulation-trade-offs.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit II

Processing Elements

Custom single purpose processor design-RT level custom single purpose processor design-optimizing custom single purpose processors-General purpose processor's software: architecture, operation, programmer's view and development environment – ASIPs - selecting a microprocessor - general purpose processor design.

9 Hours

Unit III

Memory

Introduction-memory write ability and storage Permanence-common memory types-composing memory-memory hierarchy and caches-advanced RAM.

9 Hours

Unit IV

Interfacing

Introduction-communication basics-microprocessor interfacing: I/O addressing, interrupts, DMA-Arbitration-multilevel bus architectures-advanced communication principles-serial protocols-parallel protocols-wireless protocols.

9 Hours

Unit V

Applications

Digital camera-washing machine-cell phones-home security systems-finger print identifiers-cruise control-printers-Automated teller machine.

9 Hours

Unit VI [$]

Standard single purpose processor's peripherals: timers, counters, watchdog timers, UART, PWM, LCD controllers, keypad controllers, stepper motor controllers, ADC and RTC.

Total: 45 Hours

Reference(s)

1. Frank Vahid and Tony Givargis, *Embedded system design: A unified hardware/Software introduction,* Third edition, John Wiley & sons, 2010
2. Wayne Wolf, *Computers as Components: Principles of Embedded Computing System Design*, Morgan Kaufman Publishers, 2008.
3. Jonathan.W.Valvano, *Embedded Microcomputer systems: Real Time Interfacing*, Third edition, cengage learning,2012
4. Santanuchattopadhyay, *Embedded system Design,* PHI Learning Pvt. Ltd., 2010
5. Steave Heath, *Embedded system Design,* Second edition, 2003
6. Daniel D. Gajski, Samar. Abdi, Andreas. Gerstlauer *Embedded system design: Modeling, synthesis and verification"*, Springer, 2009

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES15 ARM PROCESSORS AND CONTROLLERS

3 0 0 3

Course Objectives

- To study the concepts of Architecture and Assembly language programming of ARM Processor.
- To study the concepts of Architectural Support for High level language and memory hierarchy.
- To study the concepts of Architectural support for system Development and Operating system.

Course Outcomes (COs)

The students will be able to

1. Analyze various types of coprocessors and design suitable co-processor interface to ARM processor.
2. Analyze floating point processor architecture and its architectural support for higher level language.
3. Identify the architectural support of ARM for operating system and analyze the function of memory Management unit of ARM.

Unit I

ARM Architecture

Abstraction in hardware design – MUO -Acorn RISC Machine – Architecture Inheritance – ARM programming model – ARM Development Tools – 3 and 5 Stage Pipeline ARM Organization – ARM Instruction Execution and Implementation – ARM Co-Processor Interface.

9 Hours

Unit II

ARM Assembly Language programming

ARM Instruction Types – data Transfer, Data Processing and Control Flow Instructions – ARM Instruction set – Co-Processor Instruction.

9 Hours

Unit III

Architectural Support for High Level Language and Memory Hierarchy

Data Types – Abstraction in software design – expressions – Loops – Functions and Procedures – Conditional Statements – use of memory- Memory size and speed – On Chip Memory – Caches Design – an example –Memory management.

9 Hours

Unit IV

Architectural support for system Development

Advantaged Microcontroller Bus Architecture – ARM memory Interface – ARM Reference Peripheral Specification – Hardware System Prototyping Tools – Emulator – Debug Architecture

9 Hours

Unit V

PIC Microcontroller

CPU Architecture – Instruction set – Interrupts – Timers – Memory – I/O port expansion – I^2C bus for peripheral chip access – A/D converter – UART.

9 Hours

Unit VI[$]

An introduction to Operating systems – ARM system Control Coprocessor – CP15 Protection unit Registers – ARM Protection unit – CP15 MMU Registers – ARM MMU Architecture – Synchronization context Switching input and output.

Total: 45 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Reference(s)

1. Steve Furber, *ARM System on Chip Architecture*, Addison –Wesley Professional, 2000.
2. Ricardo Reis, *Design of System on a Chip: Devices and Components*, Springer, 2004.
3. Jason Andrews, o-*Verification of Hardware and Software for ARM System on Chip Design (Embedded Technology*), ewnes, BK and CD-ROM, Aug 2004.
4. P.Rashinkar, L.Paterson and Singh, *System on a Chip Verification- Methodologies and Techniques*, Kluwer Academic Publishers, 2000.

15ES17 PROCESSORS AND CONTROLLERS LABORATORY

0 0 2 1

Course Objectives

- To focus on the embedded system hardware development.
- To implement and simulate assembly language and C programs.
- To analyze system performance using different processing units.

Course Outcomes (COs)

The student will be able to

1. Programming an embedded system with a combination of C and assembly language.
2. Have knowledge about the applications of embedded systems.
3. Designing embedded system hardware with specific sensors and actuators.

List of Experiments (PIC/ARM/ColdFire)

1. Study of Trainer kit and IDE
2. Interface switches and LEDs
3. Interfaced and display “Hello World”
4. Interface 4*4 matrix keyboard
5. Interface stepper motor
6. Implementation of Interrupt Handling Techniques.
7. Interface 7 Segment Display using I2C
8. Serial communication using UART to display “Hello World” in PC
9. Interface LM35 temperature sensor using ADC
10. Generation of RAMP wave using on-chip DAC
11. Implementation of device drivers
12. Hands-on Project work

Total: 30 Hours

15ES18 EMBEDDED OPERATING SYSTEMS LABORATORY

0 0 2 1

Course Objectives

- To understand the fundamental concepts of operating systems.
- To understand the principles of concurrency and synchronization and apply them to write correct concurrent programs
- To understand the basic resource management techniques in an operating system

Course Outcomes (COs)

The student will be able to

1. Understand the design aspects of operating system.
2. Explain the concepts of process, address space, and file.
3. Compare and contrast various CPU scheduling algorithms.

List of experiments

1. Estimation of execution time of a program.
2. Design of priority based scheduling
3. Multi task handling using polled loop and interrupt methods.

4. Writing Multithreaded S/W
5. Manipulating Kernel Objects
6. Developing an Application using Inter Process Communication
7. Implementation of Offline Scheduling
8. Implementation of Online Scheduling
9. Implementation a semaphore for task switching
10. Implementation of thread synchronization
11. Mini-project

Total: 30 Hours

15GE19 BUSINESS ENGLISH - I

1 0 2 2

Course Objectives

- To acquire skills for using English in workplace effectively.
- To communicate for essential business needs.
- To prepare students for taking BEC Vantage level examination which is an International Benchmark for English language proficiency of Cambridge English Language Assessment (CELA).

Course Outcomes (COs)

1. To enable students to get International recognition for work and study.
2. To use English confidently in the International business environments.
3. To be able to take part in business discussion, read company literature, write formal and informal business correspondences and listen and understand business conversations.

UNIT I
GRAMMAR AND VOCABULARY

Comparison of adjectives – forming questions – asking complex questions – expressing purpose and function – tenses – conditionals – time statements – modal verbs – active and passive voice – articles – direct and indirect speech – cause and effect – relative pronouns – expressions followed by – *ing* forms – countable / uncountable – acronyms – marketing terms / vocabulary – financial terms – collocations – discourse markers.

10 Hours

UNIT II
LISTENING

Purposes of listening – features of listening texts – potential barriers to listening – specific listening skills – strategies to use when listening– distinguishing relevant from irrelevant information – gap filling exercise – multiple-choice options – note completion – matching and multiple choice questions – listening for specific information, gist, topic, context and function.

7 Hours

UNIT III
SPEAKING

Word and sentence stress – clear individual sounds – turn taking – initiating and responding - intonation patterns – pronunciation – mother tongue intrusion– conversation practice – turn-taking and sustaining the interaction by initiating and responding appropriately.

10 Hours

UNIT IV
READING

Purposes of reading – potential barriers to reading – paraphrasing – identifying facts and ideas – skimming and scanning for information – matching statements with texts– spotting reference words – understanding text structure – understanding the ideas in a text – distinguishing between the correct answer and the distractor – understanding cohesion in a text – deciphering contextual meaning of words and phrases – cloze – proof reading - transcoding.

8 Hours

UNIT V
WRITING
Paragraphing a text – using appropriate connectives – editing practice –Longer Documents: writing a proposal.

10 Hours
Total: 45 Hours

Reference(s)
1. Guy Brook-Hart, "BEC VANTAGE: BUSINESS BENCHMARK Upper-Intermediate – Student's Book", 1st Edition, Cambridge University Press, New Delhi, 2006.
2. Cambridge Examinations Publishing, "Cambridge BEC VANTAGE – Self-study Edition", Cambridge University Press, UK, 2005.

15ES21 RESEARCH METHODOLOGY

3 0 0 3

Course Objectives
- To import the knowledge on analysis of Research methodology
- The students will be able to estimate the performance of different testing method for research.

Course Outcome (Cos)
1. The Students will be able to analysis the methods used for data collection hypothesis testing and sampling process for research methodology

Unit I
Introduction
Definition, mathematical tools for analysis, Types of research, exploratory research, conclusive research, modeling research, algorithmic research, Research process- steps.
Data collection methods- Primary data – observation method, personal interview, telephonic interview, mail survey, questionnaire design. Secondary data- internal sources of data, external sources of data.

9 Hours

Unit II
Sampling Methods
Scales – measurement, Types of scale – Thurstone's Case V scale model, Osgood's Semantic Differential scale, Likert scale, Q- sort scale. Sampling methods- Probability sampling methods – simple random sampling with replacement, simple random sampling without replacement, stratified sampling, cluster sampling. Non-probability sampling method – convenience sampling, judgment sampling, quota sampling.

9 Hours

Unit III
Hypotheses Testing
Testing of hypotheses concerning means -one mean and difference between two means -one tailed and two tailed tests, concerning variance – one tailed Chi-square test.

9 Hours

Unit IV
Research in Embedded Systems
Embedded System: Scope – Economics Stakes – Trends – State of Art – Examples: Air Traffic control – The Next Generation: Technological challenges – Scientific challenges - Cost.

9 Hours

Unit V
Challenges
Physical Systems Engineering: Analytical Models – Computing Systems Engineering: Computational Models – Proposed Vision: Multidisciplinary Integration – Sub – Challenge: Integrate Analytical and Computational Models.

9 Hours

Unit VI[$]

Case Study: apply Research Methodology principles into design and manufacturing field.

Total: 45 Hours

References

1. 1. Kothari, C.R., *Research Methodology –Methods and techniques*, New Age Publications, New Delhi, 2009.
2. Panneerselvam, R., *Research Methodology*, Prentice-Hall of India, New Delhi, 2004.

15ES22 REAL TIME OPERATING SYSTEMS

3 2 0 4

Course Objectives

- To acquire knowledge about different types of scheduling algorithms
- To study about microC/OSII RTOS
- To understand the various functions of RTOS

Course Outcomes (COs)

The student will be able to

1. Describe the general architecture of computers.
2. Describe, contrast and compare differing structures for operating systems.
3. understand and analyze theory and implementation of processes, resource control (concurrency etc.), physical and virtual memory, scheduling, I/O and files.

Unit I

Basic Principles & tasks

Basic Principles - Operating System structures - System Calls - Files-Processes - Design and Implementation of processes - Communication between processes - Introduction to Distributed operating system - Distributed scheduling - Real time computation - structure of a real system - task classes - performance measures for real time systems - estimating program run times - task assignment and scheduling - classicaluni-processor scheduling algorithms - task assignment.

9 Hours

Unit II

Real Time Models

Event-based, process-based and graph-based models, petrinet models - real time languages - system performance analysis - optimization of time loading and memory loading models of multi processor system and distributed systems - task assignment - end to end tasks in heterogeneous systems - temporal distance constraints - resource contention - resource access control - priority ceiling - multiple unit resource access - access to data objects - concurrency.

9 Hours

Unit III

RTOS Concept

Fore ground and back ground process - resources - tasks - multi tasking – priorities - schedulers - kernel - exclusion - inter-task communication - interrupts - clock tick - microC/OS II kernel structure - microC/OS II initialization - starting MicroC/OS II RTOS Functions: task management - time management - semaphore management - mutual exclusion - semaphore -event management - message management - memory management - porting microC/OSII.

9 Hours

Unit IV

RTOS Functions

Task Management - Time management - Semaphore Management - Mutual Exclusion - Semaphore - Event Management - Memory Management - Porting microC/OS II.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit V

Real Time Kernel and RTOS Applications

Principles - design issues - polled loop systems - RTOS porting to a target - comparison between multitasking OS, embedded OS and RTOS- RTOS for image processing - embedded RTOS for VOIP- RTOS for fault-tolerant application - RTOS for control systems.

9 Hours

Unit VI[$]

I/O Management and Disk Scheduling: I/O Devices, Organization of I/O functions, Operating System Design issues, I/O Buffering, Disk Scheduling (FCFS, SCAN, C-SCAN, SSTF), Disk Caches.

Total: 45+30 Hours

Reference(s)

1. Philip Laplante, *Real Time Design and Analysis-an Engineer's hand book*, Wiley IEEE Press, 2004
2. C.M. Krishna and Kang Shin, *Real Time Systems*, McGraw Hill, 2001
3. Jean Labrosse, *Micro C/OS II-Real Time Kernel*, CMP Books, 2002
4. Silberschatz, P. B. Galvin, and G. Greg, *Operating System Concepts*, Wiley Publications, 2002
5. P. C. P. Bhatt, *Operating Systems*, NPTEL Courseware.

15ES23 EMBEDDED SYSTEMS ARCHITECTURE

3 2 0 4

Course Objectives

- To explore the concepts of Multi-rate signal processing by study DFT, Computation and design of Multi rate filters.
- To study the adaptive filters and its applications.
- To establish fundamental concepts on signal processing in modern spectral estimation.

Course Outcomes (COs)

The student will able to

1. Exposure with different families and architectures of Embedded System tools such as ARM Microcontrollers, DSPs/FPGAs etc.
2. Design any embedded system (h/w or s/w or both) based on any of the above tools.
3. Expertise themselves in Embedded Software particularly in real-time programming with Industry standard RTOS such as VxWorks and RTLinux.

Unit I

Embedded Systems Architecture & Models

Introduction to Embedded Systems Architecture - Embedded Systems Model - - Product specification – Hardware / Software partitioning - Identifying software and hardware elements - Determining optimal partitioning between software and hardware

9 Hours

Unit II

Embedded Hardware

ISA Architecture Models - internal Processor Design - Processor Performance - Board Memory – Memory Management of External Memory - Board I/O: Serial vs. Parallel I/O - Interfacing the I/O Components - I/O and Performance.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit III

Embedded Software

Device Drivers: Device Drivers for Interrupt-Handling - Memory Device Drivers - board Bus - Device Drivers - OS Performance Guidelines - OS and Board Support Packages - Middleware and Application Software

9 Hours

Unit IV

Design and Development

Embedded System Architecture: Architecture Business Cycles -Architectural Patterns and Reference Models – Architectural structures – Document, Analyze and Evaluate the OS Architecture

9 Hours

Unit V

Implementation and Testing

Implementing the Design - Writing Code in an Editor - CAD and the Hardware- Debugging Tools - System Boot-Up - Quality Assurance and Testing of the Design

9 Hours

Unit VI[$]

Board Buses: Bus Arbitration and Timing - Integrating the Bus with Other Board Components - Bus Performance

Total: 45+ 30 Hours

Reference(s)

1. Tammy Noergaard, *Embedded Systems Architecture*, Elsevier, 2005.
2. Wayne Wolf, *Computers as Components: Principles of Embedded Computing System Design*, Morgan Kaufman Publishers, 2008.
3. Arnold Berger, *Embedded systems Design*, CMP Books, 2003.

15ES24 SOFTCOMPUTING TECHNIQUES

3 2 0 4

Course Objectives

- To expose the concepts of feed forward neural networks.
- To provide adequate knowledge about feedback neural networks.
- To teach about the concept of fuzziness involved in various systems.
- To expose the ideas about genetic algorithm

Course Outcomes (COs)

The student will be able to

1. Apply derivative based and derivative free optimization.
2. Demonstrate some applications of computational intelligence
3. Analyze and model computer systems specific problems, identify and define the appropriate requirements for their solutions.

Unit I

Introduction of Soft Computing

Introduction of soft computing - soft computing vs. hard computing- various types of soft computing techniques- applications of soft computing-Neuron- Nerve structure and synapse- Artificial Neuron and its model- activation functions.

9 Hours

Unit II

Introduction to Artificial Neural Networks

Neural network architecture- single layer and multilayer feed forward networks- McCullochPitts neuron model- perceptron model- Adaline and Madaline- multilayer

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

perception model- back propogation learning methods- effect of learning rule coefficient - back propagation algorithm- factors affecting back propagation training –applications.

9 Hours

Unit III

Artificial Neural Networks

Counter propagation network- architecture- functioning & characteristics of counter-Propagation network-Hopfield/ Recurrent network- configuration- stability constraints-associative memory- and characteristics- limitations and applications- Hopfield v/s Boltzman machine- Adaptive Resonance Theory- Architecture- classifications-Implementation and training-Associative Memory.

9 Hours

Unit IV

Fuzzy Logic System

Introduction to crisp sets and fuzzy sets- basic fuzzy set operation and approximate reasoning. Introduction to fuzzy logic modeling and control- Fuzzification- inferencingand defuzzification-Fuzzy knowledge and rule bases-Fuzzy modeling and control schemes for nonlinear systems. Self organizing fuzzy logic control- Fuzzy logic control for nonlinear time delay system.

9 Hours

Unit V

Genetic Algorithm

Basic concept of Genetic algorithm and detail algorithmic steps-adjustment of free Parameters-Solution of typical control problems using genetic algorithm- Concept on some other search techniques like tabu search and ant colony search techniques for solving optimization problems.

9 Hours

Unit VI[$]

Variants of Binary Encoded Genetic Algorithms: Micro Genetic Algorithm, Messy Genetic Algorithm, Greedy Genetic Algorithm etc. and their usage in Engineering Problems.

Total: 45+30 Hours

Reference(s)

1. Laurene V. Fausett, Fundamentals of Neural Networks: Architectures, Algorithms & Applications, Pearson Education, 2009
2. Timothy J. Ross, “Fuzzy Logic with Engineering Applications” Wiley India.2008
3. Zimmermann H.J. "Fuzzy set theory and its Applications" Springer international edition, 2011.
4. David E.Goldberg, “Genetic Algorithms in Search, Optimization, and Machine Learning”, Pearson Education,2009.
5. W.T.Miller, R.S.Sutton & P.J.Webrose, “Neural Networks for Control”, MIT Press, 1996.

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES27 REAL TIME OPERATING SYTEMS LABORATORY

0 0 2 1

Course Objectives

- To study the design of ARM, PIC, VLSI and DSP based embedded system design.
- To complete the design of an embedded system with functional requirements for hardware and software components including processor, networking components, and sensors, along with applications, subsystem interfaces, networking, and middleware.
- To implement a subsystem and integrate this with a complete system to perform a complex task involving networked, mobile embedded systems.

Course Outcomes (COs)

1. Develop an embedded system project concept.
2. Develop a design specification.
3. Create a development plan covering such items as functional description, implementation methods, resource, requirements, schedule, and interface requirements, integration strategy, and test plan.

List of Experiments

Implement one of the real world examples from the following domains:

1. Embedded systems for an elevator control.
2. Embedded systems for a camera – Range of cameras from low cost to fast expensive Movie camera.
3. Embedded systems for Set Top Box solutions.
4. Embedded systems for Unmanned air vehicle (UAV).
5. Integrated systems for Warfield equipment: Radar, Battle Tank, GUN Control systems.
6. Wireless sensor network.
7. Intelligent Building.
8. Smart Substations and smart Grid solutions.
9. Highly intelligent access and authentication stations.

Total: 30 Hours

15ES28 TECHNICAL SEMINAR

0 0 2 1

15GE29 BUSINESS ENGLISH - II

1 0 0 1

Course Objective

- To acquire skills for using English in business environment.
- To communicate appropriately in business contexts.
- To prepare students for taking BEC Vantage level examination conducted by the Cambridge English Language Assessment (CELA).

Course Outcome (COs)

1. To enable students to acquire business terms for communication.
2. To use English confidently in the business contexts.
3. To be able to take part in business discussion and write formal and informal business correspondences.

UNIT I

SPEAKING

Non-verbal communication – agreeing / disagreeing, reaching decisions, giving and supporting opinions – making mini presentations – extending on conservations – collaborative task – tongue twisters.

6 Hours

UNIT II
WRITING
Business letters – fax – Shorter Documents: e-mail - memo – message - note – report writing – formal / informal styles.

9 Hours
Total: 15 Hours

Reference Books:
1. Guy Brook-Hart, "BEC VANTAGE: BUSINESS BENCHMARK Upper-Intermediate – Student's Book", 1st Edition, Cambridge University Press, New Delhi, 2006.
2. Cambridge Examinations Publishing, "Cambridge BEC VANTAGE – Self-study Edition", Cambridge University Press, UK, 2005.

15ES51 MULTIPROCESSOR

3 0 0 3

Course Objectives
- To Learn parallel computer architectures with multiprocessor and multi-core
- To understand Master parallel programming techniques
- To gain experiences of applying parallel programming to achieve performance gains from multiprocessor and multi-core computer systems.

Course Outcomes (COs)
The student will be able to
1. Understand the advanced concepts of computer architecture.
2. Investigating modern design structures of Pipelined and Multiprocessors systems.
3. Become acquainted with recent computer architectures and I/O devices, as well as the low-level language required to drive/manage these types of advanced hardware.

Unit I
Application-Specific Multiprocessors
Parallel architecture classifications - Exploiting instruction-level parallelism - Dataflow DSP architectures - Systolic and wavefront arrays - Multiprocessor DSP architectures - Single-chip multiprocessors , Terminology: Graph data structures - Dataflow graphs - Computation graphs - Petri Nets - Synchronous dataflow – SDF and Expansion graphs - Synchronous languages - HSDFG concepts and notations - Complexity of algorithms - Maximum cycle mean

9 Hours

Unit II
Dataflow and Scheduling Models
Dataflow Models: Scalable synchronous, Cyclostatic, Multidimensional synchronous, Parameterized dataflow models - Reactive process networks - Integrating dataflow and state machinemodels - Controlled dataflow actors , Scheduling Models: Task-level parallelism and data parallelism, Static versus dynamic scheduling strategies, Fully static, Self-timed, Dynamic, Quasi-static, schedules, Scheduling Algorithms : Stone's assignment algorithm, List scheduling algorithms, Clustering algorithms, Integrated scheduling algorithms, Pipelined scheduling

9 Hours

Unit III
Ordered-Transactions Strategy
Shared bus architecture – Inter-processor communication mechanisms - Design of an ordered memory access multiprocessor - Design details of a prototype - Hardware and software implementation - Ordered I/O and parameter control – Inter-processor communication graph (Gipc) - Execution time estimates - Ordering constraints viewed as added edges - Periodicity - Optimal order - Effects of changes in execution times - Effects of inter-processor communication costs - Application examples

9 Hours

Unit IV

Synchronization

The barrier MIMD technique - Redundant synchronization removal in non-iterative dataflow - Analysis of self-timed execution - Strongly connected components and buffer size bounds - Synchronization model - A synchronization cost metric - Removing redundant synchronizations - Insertion of delays – Definition, properties of resynchronization - Relationship to set covering - Intractability of resynchronization - Heuristic solutions - Chainable synchronization graphs - Resynchronization of constraint graphs for relative scheduling - Elimination of synchronization edges – LCR - Intractability of LCR - Two-processor systems - A heuristic for general synchronization graphs - Integrated Synchronization Optimization

9 Hours

Unit V

Run Time System

Exceptions, Interrupts, and Traps - Application Binary Interface Considerations - Loading Programs - Data Layout -Accessing Global Data - Calling Conventions - Advanced ABI Topics - Code Compression - Multiprocessing and Multithreading

9 Hours

Unit VI[$]

General concepts of Application specific Instruction set processor (ASIP)- Application of ordered transaction strategy and examples - Integrated Synchronization Optimization - Special considerations in an RTOS.

Total: 45 Hours

Reference(s)

1. Sunderrajan Sriram and Shuvra S Battacharya, *Embedded Multiprocessos Scheduling and Synchronization*, Marcel Dekker Incorporated, 2002.
2. Joseph A Fisher, Polo Faraboschi, CliffYoung, *Embedded Computing: A VLIW Approach to Architecture*, Elseiver Publications, 2008
3. Maurice Herlihy, NirShavit, *The Art of Multiprocessor Programming*, Morgan Kaufmann, 1st edition, 2008.

15ES52 / 15CO13/15AE55 STATISTICAL SIGNAL PROCESSING
(Common to Communication Systems, Applied Electronics & Embedded Systems)

3 0 0 3

Course Objectives

- To explore the concepts of multi rate signal processing and multi rate filters.
- To study the adaptive filters and its applications.
- To learn fundamental concepts on signal processing in power spectrum estimation.

Course Outcomes (COs)

The student will be able to

1. Acquiring knowledge of how a multi rate system works.
2. Ability to design and implement decimator and interpolator and to design multi rate filter bank.
3. Understanding different spectral estimation techniques and linear prediction.
4. Ability to design LMS and RLS adaptive filters for signal enhancement, channel equalization.

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit I

Multirate signal Processing

Introduction-Sampling and Signal Reconstruction-Sampling rate conversion – Decimation by an integer factor – interpolation by an integer factor –Sampling rate conversion by a rational factor – poly-phase FIR structures – FIR structures with time varying coefficients - Sampling rate conversion by a rational factor- Multistage design of decimator and interpolator.

9 Hours

Unit II

Multirate FIR Filter Design

Design of FIR filters for sampling rate conversion –Applications of Interpolation and decimation in signal processing –Filter bank implementation –Two channel filter banks-QMF filter banks – Perfect Reconstruction Filter banks – tree structured filter banks - DFT filter Banks – M-channel filter banks- octave filter banks

9 Hours

Unit III

Linear Estimation and Prediction

Linear prediction- Forward and backward predictions, Solutions of the Normal equations- Levinson-Durbin algorithms. Least mean squared error criterion -Wiener filter for filtering and prediction, FIR Wiener filter and Wiener IIR filters ,Discrete Kalman filter.

9 Hours

Unit IV

Adaptive Filters

FIR Adaptive filters - Newton's steepest descent method – Adaptive filters based on steepest descent method - LMS Adaptive algorithm – other LMS based adaptive filters- RLS Adaptive filters - Exponentially weighted RLS - Sliding window RLS - Simplified IIR LMS Adaptive filter.

9 Hours

Unit V

Power Spectral Estimation

Estimation of spectra from finite duration observations of a signal –The Periodogram-Use of DFT in Power spectral Estimation –Non-Parametric methods for Power spectrum Estimation – Bartlett. Welch and Blackman–Tukey methods –Comparison of performance of Non – Parametric power spectrum Estimation methods –Parametric Methods - Relationship between auto correlation and model parameters, Yule-Walker equations, solutions using Durbin's algorithm,AR, MA, ARMA model based spectral estimation.

9 Hours

Unit VI[$]

Applications of adaptive filters: Adaptive channel equalization Adaptive echo canceller - Adaptive noise cancellation-, 1/M octave-band filter banks, Speech enhancement using spectrum estimation

Total: 45 Hours

Reference(s)

1. H. Monson Hayes, *Statistical Digital Signal Processing and Modeling*, John Wiley and Sons, Inc., 2008.
2. G.. John Proakis and G. Dimitris Manolakis, *Digital Signal Processing*, Pearson Education, 2006.
3. P.P.Vaidyanathan , *Multirate Syatems and Filter Banks*, Pearson Education, 2008.
4. N.J.Filege, *Multirate Digital Signal Processing*, John Wiley and Sons, 2000.
5. G..John Proakis, *Algorithms for Statistical Signal Processing*, Pearson Education, 2002.

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

6. G.Dimitris and G.Manolakis., *Statistical and Adaptive Signal Processing*, McGraw Hill, 2002.
7. Sophoncles J. Orfanidis, *Optimum Signal Processing*, McGraw Hill, 2007.

15ES53/15VL68 EMBEDDED NETWORKING
(Common to Embedded Systems & VLSI Design)

3 0 0 3

Course Objective

- To study the fundamentals of embedded networking.
- To understand about the design methodologies in wireless networks.
- To Understand the basics of Ethernet and Embedded Ethernet.

Course Outcomes (COs)

The student will be able to

1. Understand the fundamentals of embedded systems programming, real-time operating systems.
2. Develop understanding of power-aware protocols for networks of small devices.
3. Explore newly established standards for embedded systems and ubiquitous computing.

Unit I

Embedded Communication Protocols

Embedded Networking: Introduction – Serial/Parallel Communication – Serial communication protocols -RS232 standard – RS485 – Synchronous Serial Protocols -Serial Peripheral Interface (SPI) – Inter Integrated Circuits (I2C) – PC Parallel port programming .

9 hours

Unit II

USB and CAN Bus

USB bus – Introduction – Speed Identification on the bus – USB States – USB bus communication: Packets –Data flow types –Enumeration –Descriptors –PIC18 Microcontroller USB Interface – C Programs –CAN Bus – Introduction - Frames –Bit stuffing –Types of errors –Nominal Bit Timing – PIC microcontroller CAN Interface .

9 hours

Unit III

Ethernet Basics

Elements of a network – Inside Ethernet – Building a Network: Hardware options – Cables, Connections and network speed – Design choices: Selecting components –Ethernet Controllers – Using the internet in local and internet communications .

9 hours

Unit IV

Embedded Ethernet

Exchanging messages using UDP and TCP – Serving web pages with Dynamic Data – Serving web pages that respond to user Input – Using FTP – Keeping Devices and Network secure.

9 hours

Unit V

Wireless Embedded Networking

Wireless sensor networks – Introduction – Applications – Network Topology – Localization – Time Synchronization - Energy efficient MAC protocols –SMAC – Energy efficient and robust routing .

9 hours

Unit VI[$]

ISA/PCI Bus protocols –Firewire - A simple application with CAN - Inside the Internet protocol - Email for Embedded Systems - Data Centric routing.

Total: 45 hours

Reference(s)

1. Frank Vahid, Givargis *Embedded Systems Design: A Unified Hardware/Software Introduction*, Wiley Publications, 2002.
2. Jan Axelson, *Parallel Port Complete*, Penram publications, 2011.
3. Dogan Ibrahim, *Advanced PIC microcontroller projects in C*, Elsevier 2008.
4. Jan Axelson *Embedded Ethernet and Internet Complete*, Penram publications, 2005.
5. Bhaskar Krishnamachari, *Networking wireless sensors*, Cambridge press 2005.

15ES54 SOFTWARE FOR EMBEDDED SYSTEMS

3 0 0 3

Course Objectives

- To expose the students to the fundamentals of embedded Programming.
- To Introduce the GNU C Programming Tool Chain in Linux.
- To study the basic concepts of embedded C and Embedded OS
- To introduce time driven architecture, Serial Interface with a case study.
- To introduce the concept of embedded Java for Web Enabling of systems.

Course Outcomes (COs)

The student will be able to

1. Understand c Programming tool chain in LINUX.
2. Differentiate time driven multi stage architecture and hardware.
3. Gain knowledge about Embedded C and Embedded JAVA.

Unit I

Embedded Programming

C and Assembly - Programming Style - Declarations and Expressions - Arrays, Qualifiers and Reading Numbers - Decision and Control Statements - Programming Process - More Control Statements - Variable Scope and Functions - C Preprocessor - Advanced Types - Simple Pointers - Debugging and Optimization – In-line Assembly.

9 Hours

Unit II

C Programming Toolchain in LINUX

C preprocessor - Stages of Compilation - Introduction to GCC - Debugging with GDB - The Make utility - GNU Configure and Build System - GNU Binary utilities - Profiling - using *gprof* - Memory Leak Detection with *valgrind* - Introduction to GNU C Library

9 Hours

Unit III

Embedded C

Adding Structure to 'C' Code: Object oriented programming with C, Header files for Project and Port, Examples. Meeting Real-time constraints: Creating hardware delays - Need for timeout mechanism - Creating loop timeouts - Creating hardware timeouts.

9 Hours

Unit IV

Time-Driven Multi-State Architecture and Hardware

Multi-State systems and function sequences: Implementing multi-state (Timed) system - Implementing a Multi-state (Input/Timed) system. Using the Serial Interface: RS232 - The Basic RS-232 Protocol - Asynchronous data transmission and baud rates - Flow control -

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Software architecture - Using on-chip UART for RS-232 communication - Memory requirements - The serial menu architecture - Examples. Case study: Intruder alarm system.

9 Hours

UNIT V

EMBEDDED JAVA

Introduction to Embedded Java and J2ME – Smart Card basics – Java card technology overview – Java card objects – Java card applets – working with APDUs – Web Technology for Embedded Systems.

9 Hours

UNIT VI[$]

Embedded OS : Basis of a simple embedded OS, Introduction to sEOS, Using Timer 0 and Timer 1, Portability issue, Alternative system architecture, Important design considerations when using sEOS.

Total: 45 Hours

Reference(s)

1. Steve Oualline, '*Practical C Programming* 3rd Edition', O'Reilly Media, Inc, 2006.
2. Stephen Kochan, "*Programming in C*", 3rd Edition, Sams Publishing, 2009.
3. Michael J Pont, "*Embedded C*", Pearson Education, 2007.
4. Zhiqun Chen, '*Java Card Technology for Smart Cards: Architecture and Programmer's Guide'*, Addison-Wesley, Professional, 2000.

15ES55 INDUSTRIAL ROBOTICS

3 0 0 3

Course Objectives

- To learn about the hardware, controls, peripheral equipment, and successful implementation of a robotic system in a flexible production environment.
- To learn factory communications
- to describe the structure of robot manipulator

Course Outcomes (COs)

1. Students will be equipped with the automation and brief history of robot and applications.
2. Students will be familiarized with the kinematic motions of robot.
3. Students will have good knowledge about robot end effectors and their design concepts.

Unit I

Introduction to Robotics

Robotic Classification, Robot Specifications, Motion – Bug and tangent algorithms, Potential Function, Road maps- Topological roadmaps, Cell decomposition – Trapezoidal and Morse cell decompositions , Sensor and sensor planning- Kinematics-Forward and Inverse Kinematics - Transformation matrix and DH transformation-Inverse Kinematics.

9 Hours

Unit II

Computer Vision

Projection - Optics, Projection on the Image Plane and Radiometry. Image Processing - Connectivity, Images-Gray Scale and Binary Images, Blob Filling, Thresholding, Histogram-Convolution - Digital Convolution and Filtering and Masking Techniques- Edge Detection - Mono and Stereo Vision.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit III

Sensors and Sensing Devices

Introduction to various types of sensor- Resistive sensors. Range sensors - LADAR (Laser Distance and Ranging, Sonar, Radar and Infra-red- Introduction to sensing - Light sensing, Heat sensing, touch sensing and Position sensing.

9 Hours

Unit IV

PLC

Building blocks of automation, Controllers – PLC- Role of PLC in Robotics & FA - Architecture of PLC - Advantages - Types of PLC - Types of Programming - Simple process control programs using Relay Ladder Logic and Boolean logic methods - PLC arithmetic functions.

9 Hours

Unit V

Factory Automation

Flexible Manufacturing Systems concept - Automatic feeding lines, ASRS, transfer lines, automatic inspection - Computer Integrated Manufacture - CNC, intelligent automation. Industrial networking, bus standards, HMI Systems, DCS and SCADA, Wireless controls**.**

9 Hours

Unit VI[$]

Inverse Kinematics - Geometric methods and Algebraic methods-SCARA robot - PUMA robot.

Total: 45 Hours

Reference(s)

1. Duda, Hart and Stork, *Pattern Recognition*, Wiley-Inter science, 2000
2. Mallot, *Computational Vision: Information Processing in Perception and Visual Behavior,* Cambridge, 2000
3. Stuart Russell and Peter Norvig, *Artificial Intelligence-A Modern Approach*, Pearson Education Series in Artificial Intelligence, 2004
4. Robert Schilling and Craig, *Fundamentals of Robotics: Analysis and Control*, Hall of India Private Limited, 2003
5. Forsyth and Ponce, *Computer Vision: A Modern Approach*, Person Education, 2003
6. Richard D Klafter, Thomas A Chmielewski, Michael Negin, *Robotics Engineering – An Integrated Approach*, Eastern Economy Edition, Prentice Hall of India P Ltd., 2006
7. Deh S R., *Robotics Technology and Flexible Automation,* Tata McGraw Hill Publishing, Company Ltd., 1994

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES56 AUTOMOTIVE NETWORKING

3 0 0 3

Course Objectives

- To focus popular standards and future data communication.
- To impart knowledge about different layers of In-vehicle protocols.
- To study the challenges and latest research results related to the In-vehicle communication protocols.

Course Outcomes (COs)

The student will be able to

1. Demonstrate a comprehensive theoretical and practical knowledge of the key elements and principles of operation of commonly used automotive networks including: CAN, MOST, LIN & FlexRay.
2. Critically analyse the suitability of different automotive networks and apply appropriate selection criteria when choosing a network technology for a particular application.
3. Evaluate the requirements and critically analyse the suitability of new automotive network technologies to support advanced safety-critical systems deployment

Unit I

Basics of In-vehicle networking

Over view of Data communication and networking –need for In-Vehicle networking –layers of OSI reference model – Overview of general purpose networks and protocols -Ethernet, TCP, UDP, IP, ICMP, ARP, vehicle buses.

9 Hours

Unit II

CAN

Overview of CAN –fundamentals –selecting CAN controller –CAN application areas–message frame formats, bit encoding –bit-timing and synchronization –data rate and bus length –network topology –bus access –physical layer standards CAN higher layer protocol- Introduction to CANopen and application in transportation electronics.

9 Hours

Unit III

LIN

LIN standard overview –applications –LIN communication- message frame formats – development flow - LIN Descriptor Files - LIN schedule

9 Hours

Unit IV

MOST and FlexRay

MOST overview –data rates –data types –topology –application areas –FlexRay introduction – network topology –ECUs and bus interfaces –controller host interface and protocol operation controls –media access control and frame and symbol processing –coding/decoding unit – FlexRay scheduling –message processing –wakeup/ startup applications

9 Hours

Unit V

Wireless systems

Introduction to wireless systems – GPS – Setting receivers – Positioning – activating the navigation function – Concept of latitude and longitude grid system - Mapping and location technologies - Application.

9 Hours

Unit VI[$]

Introduction to CAN open and application in transportation electronics - wakeup/ startup applications in MOST - Application of wireless system.

Total: 45 Hours

Reference(s)

1. B.Hoffman – Wellenhof, H.Lichtenegger and J.Collins, "*GPS Theory and practice*". 4th revised edition, Springer, Wein, New York, 1997
2. IndraWidjaja, Alberto Leon-Garcia*, "Communication Networks: Fundamental Concepts and Key Architectures"*, McGraw-Hill College 1st edition, January 15, 2000.
3. Konrad Etschberger, "*Controller Area Network"*, IXXAT Automation, August 22, 2001.
4. Olaf Pfeiffer, Andrew Ayre, Christian Keydel, "*Embedded Networking with CAN and CANopen*," Annabooks/Rtc Books, November 1, 2003
5. Ronald K Jurgen, "*Automotive Electronics Handbook",* McGraw-Hill Inc., 1999.
6. Dennis Foy, "*Automotive Telematics",* Red Hat, 2002
7. Ronald K Jurgen,, "*Automotive microcontrollers",* Society of Automotive Engineers Inc., 1998

15ES57 IMAGE PROCESSING TECHNIQUES

3 0 0 3

Course Objectives

- To study about the fundamentals of digital images.
- To understand 1D and 2D image transforms.
- To gain sound knowledge about various image processing techniques.

Course Outcomes (COs)

The students will be able to

1. Understand image formation and the rolehumanvisual system plays in perception of gray and color image data.
2. Learn the signal processingalgorithms and techniques in image enhancement and image restoration.
3. Acquire an appreciation for the image processing issues and techniques and be able to applythese techniques to real world problems.

Unit I

Digital Image Fundamentals

Elements of digital image processing systems - Elements of visual perception - psycho visual model – brightness – contrast – hue – saturation - mach band effect –Image sensing and acquisition- Image sampling and Quantization –Basic relationships between pixels- Two-dimensional mathematical preliminaries.

9 Hours

Unit II

Image Transforms

Analysis of 1D DFT - 2D transforms – DFT – Discrete Cosine Transform - Discrete Sine Transform – Walsh – Hadamard – Slant – Haar- KLT – SVD - Wavelet Transform.

9 Hours

Unit III

Image Enhancement and Restoration

Basic Gray Level Transformations - Histogram Processing - Smoothing and Sharpening Spatial Filters- Smoothing and Sharpening Frequency Domain Filters - Homomorphic filtering- Image degradation/ restoration process model – Noise models- Restoration in the presence of noise only

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Spatial Filtering- Inverse filtering –Wiener filtering - Geometric transformations.

9 Hours

Unit IV

Image Segmentation and Recognition

Edge detection - edge linking – Basic global and adaptive thresholding - Image segmentation by region growing - region splitting and merging - Image Recognition – Patterns and pattern classes - Matching by minimum distance classifier - Back Propagation Neural Network - Neural Network applications in image processing.

9 Hours

Unit V

Image Compression

Need for data compression – Image Compression models- Huffman - Run Length Encoding - Arithmetic coding - Vector Quantization - Block Truncation Coding - Transform Coding – Wavelet coding-Image Compression Standards – Introduction to fractal image compression.

9 Hours

Unit VI[$]

Image understanding – Video motion analysis – Image fusion – Steganogaphy – Colour image processing.

Total: 45 Hours

Reference(s)

1. C.Rafael Gonzalez and E. Richard Woods, *Digital Image Processing*, Pearson Education Inc., 2004.
2. David Salomon, *Data Compression – The Complete Reference*, Springer, 2001.
3. K.William Pratt, *Digital Image Processing*, John Wiley, 2002.
4. MilmanSonka, Vaclav Hlavac and Roger Boyle, *Image Processing, Analysis, and Machine Vision*, Brooks/Cole, Vikas Publishing House, 2007.
5. Anil K. Jain, *Fundamentals of Digital Image Processing*, Prentice Hall of India, 2002.

15ES58 HARDWARE DESCRIPTION LANGUAGE

3 0 0 3

Course Objectives

- To understand the Concepts of Verification Techniques and Tools.
- To study the concepts of Verification Plan, Stimulus and Response.
- To understand the concepts of Architecting Test benches and System Verilog.

Course Outcomes(COs)

The students will be able to

1. Develop program codes for structural and behavioral modeling of combinational and sequential logic using Verilog HDL in any problem identification, formulation and solution.
2. Describe the role of hardware description language (HDL) in design flows for FPGA with a historical development of the Verilog HDL.
3. Learn to analyze the problems in digital design using HDLs.

Unit I

Basic Concepts of Hardware Description Language

Comparison between HDL and High Level Language Hierarchy, Concurrency, Logic and Delay Modeling, Structural, Data flow, Behavioral Styles of Hardware Description, Architecture of event driven simulation.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit II
VHDL
Data Types, Operators, Classes of Objects, entities and architectures, Attributes – concurrent statements – sequential statements – signals and variables – Behavior, dataflow and structural modeling – Configurations, functions – procedures – packages – test benches – Design examples
9 Hours

Unit III
Verilog
Signals, Identifier Names, Net and Variable Types, operators, Gate instantiations, Verilog module, concurrent and procedural statements, UDP, sub circuit parameters, function and tasks – test benches – Design Examples
9 Hours

Unit IV
Timing Issues
Modeling delay, Timing Modeling, Timing Assertion, Setup and hold times for clocked devices.
9 Hours

Unit V
System Modeling
Processor model, RAM model, UART model, Interrupt Controller.
9 Hours

Unit VI[$]
Verilog and VHDL programs for sequential circuits – Synchronous Circuits – Asynchronous Circuits- ASM.
Total: 45 Hours

Reference(s)
1. J.Bhasker, A VHDL Primer, Prentice Hall, 1998.
2. J.Bhasker, VHDL Synthesis Primer, Prentice Hall.1998.
3. J.Bhasker, A Verilog Primer, Prentice Hall 2005.
4. Michel D Ciletti, Advanced Digital Design with Verilog HDL, Pearson education, 2010.
5. Volnei A Pedroni , Circuit Design with VHDL, Prentice Hall, 2004.
6. Samir Palnitkar, Verilog HDL a Guide to Digital Design and Synthesis, Prentice Hall NJ,USA, 1996.

15ES59 INFORMATION THEORY AND CODING

3 0 0 3

Course Objectives
- To define and apply the basic concepts of information theory
- To differentiate between lossy and lossless data compression methods, and describe the most common such methods
- To calculate the capacity of communication channels

Course Outcomes (COs)
The student will be able to
1. Analyse the fundamental parameters relevant to information theory
2. Explain and analyse source coding, compression and error control methods
3. Calculate the channel capacity of simple noisy channels including the binary symmetric case, and interpret the result in terms of theoretical limits to channel coding performance.

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit I

Information theory

Concept of amount of information -units, Entropy -marginal, conditional and joint entropies - relation among entropies Mutual information, information rate, channel capacity, redundancy and efficiency of channels.

9 Hours

Unit II

Discrete channels

Symmetric channels, Binary Symmetric Channel, Binary Erasure Channel, Cascaded channels, repetition of symbols, Binary unsymmetric channel, Shannon theorem. Continuous channels – Capacity of band limited Gaussian channels, Shannon-Hartley theorem, Tradeoff between band width and signal to noise ratio, Capacity of a channel with infinite band width, Optimum modulation system.

9 Hours

Unit III

Source coding

Encoding techniques, Purpose of encoding, Instantaneous codes, Construction of instantaneous codes, Kraft's inequality, Coding efficiency and redundancy, Noiseless coding theorem. Construction of basic source codes – Shannon-Fano algorithm, Huffman coding, Arithmetic coding, ZIP coding**.**

9 Hours

Unit IV

Error detection and correction

Parity check coding, Linear block codes, Error detecting and correcting capabilities, Generator and Parity check matrices, Standard array and Syndrome decoding, Hamming codes, Encoding and decoding of systematic and unsystematic codes. Cyclic codes – Generator polynomial, Generator and Parity check matrices, Encoding of cyclic codes, Syndrome computation and error detection, Decoding of cyclic codes, BCH codes, RS codes, Burst error correction.

9 Hours

Unit V

Convolutional codes

Encoding- State, Tree and Trellis diagrams, Maximum likelihood decoding of convolutional codes -Viterby algorithm, Sequential decoding -Stack algorithm. Interleaving techniques – Block and convolutional interleaving, Error Control and Signal Space Coding

9 Hours

Unit VI[$]

Lloyd-Max Quantizer-Companded Quantization- Vector Quantization-Transform Coding Part I&Part II-Differential entropy-Application of information theories.

Total: 45 Hours

Reference(s)

1. Simon Haykin, *Communication Systems*, John Wiley & Sons. Pvt. Ltd., 2009
2. Taub& Schilling, *Principles of Communication Systems*, Tata McGraw-Hill, 2007.
3. J.Das, S.K. Mullick and P.K. Chatterjee, *Principles of Digital Communication*, Wiley Eastern Ltd., 2002
4. Shu Lin & Daniel J. Costello Jr., *Error Control Coding Fundamentals and Applications,* Prentice Hall Inc., 2004
5. Graham Wade, *Coding Techniques*, Palgrave Publishers, 2000.
6. Thomas and Joy A Thomas, *Elements of Information Theory*, John Wiley India Inc., 2008
7. Fazlollah M. Reza,*An Introduction to Information Theory,* Dover Edition 1994

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES60 / 15VL53 SYSTEM ON CHIP
(Common to Embedded Systems & VLSI Design)

3 0 0 3

Course Objectives

- To understand the concepts of System on Chip Design methodology for Logic and Analog Cores.
- To understand the concepts of System on Chip Design Validation.
- To understand the concepts of SOC Testing.

Course Outcomes (Cos)

The student will be able to

1. Understand all important components of a System-on-Chip and an embedded system, i.e. digital hardware, analog hardware and embedded software
2. Understand the major architectures and trade-offs concerning performance, cost and power consumption of single chip and embedded explain the role of protocols in networking.
3. Know the major design flows for digital hardware, analog hardware and embedded software

Unit I

Introduction of Chip

System tradeoffs and evolution of ASIC Technology- System on chip concepts and methodology – SoC designissues -SoC challenges and components.

9 Hours

Unit II

Design Methodological For Logic Cores

SoC Design Flow – On-chip buses –Design process for hard cores –Soft and firm cores – Designing with hard cores, soft cores- Core and SoC design examples.

9 Hours

Unit III

Design Methodology for Memory and Analog Cores

Embedded memories –Simulation modes Specification of analog circuits – A to D converter – Phase- locatedloops –High I/O.

9 Hours

Unit IV

Design Validation

Core level validation –Test benches –SoC design validation – Co simulation –hardware/ Software co-verification. Case Study: Validation and test of systems on chip

9 Hours

Unit V

Soc Testing

SoC Test Issues – Testing of digital logic cores –Cores with boundary scan –Test methodology for design reuse– Testing of microprocessor cores – Built in self method –testing of embedded memories.

Case Study: Integrating BIST techniques for on-line SoC testing.

9 Hours

Unit VI[$]

Designing BIST techniques for SOC testing- soft core models for different logic circuits

Total: 45 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Reference(s)

1. RochitRajsunah, *System-on-a-chip: Design and Test*, Artech House, 2007.
2. PrakashRaslinkar, Peter Paterson &Leena Singh, *System-on-a-chip verification: Methodology andTechniques*, Kluwer Academic Publishers, 2000.
3. M.Keating, D.Flynn, R.Aitken, A, GibbonsShi, *Low Power Methodology Manual for System-on-ChipDesign Series: Integrated Circuits and Systems*, Springer, 2007.
4. L.Balado, E. Lupon, *Validation and test of systems on chip*, IEEE conference on ASIC/SOC,1999.
5. A.Manzone, P.Bernardi, M.Grosso, M. Rebaudengo, E. Sanchez, M.SReorda, Centro Ricerche Fiat, *Integrating BIST techniques for on-line SoC testing*, IEEE Symposium on On-line testing *2005.*
6. Wang, Charles E Strout and NurATouba, *System on Chip Test Architectures: Nanometer Design for Testability*, Morgan Kaufmann, 2007.

15ES61 LOW POWER VLSI DESIGN

3 0 0 3

Course objectives

- To understand the different types of low power adders and multipliers
- To focus on synthesis of different level low power transforms.
- To gain knowledge on low power static RAM architecture & the source of power dissipation in SRAM

Course Outcomes (COs)

The student will be able to

1. Able to understand the different techniques involved in low power adders and multipliers
2. Understandings of the impact of various low power transform
3. Identify and analyze the different techniques involved in low power SRAM.

Unit I

Power Dissipation in CMOS

Sources of power Dissipation–Physics of power dissipation in MOSFET devices, Power dissipation in CMOS, Power dissipation in Domino CMOS-Low power VLSI design limits.

9 Hours

Unit II

Power Estimation

Modeling of signals- Signal probability calculation-probabilistic techniques for signal activity estimation-statistical techniques for power estimation-estimation of glitch power-sensitivity analysis-power estimation at the circuit level-estimation of maximum power.

9 Hours

Unit III

Synthesis for Low power

Behavioral level transforms-Algorithm using First –Order, second, M^{th} Order Differences-Parallel Implementation Pipelined Implementation- Logic level optimization– Technology dependent and Independent– -Circuit level-Static, Dynamic, PTL,DCVSL,PPL.

9 Hours

Unit IV

Low power static RAM Architectures

Organization of a static RAM, MOS static RAM memory cell, Banked organization of SRAMs, Reducing voltage swings on bit lines, Reducing power in the write diver circuits, Reducing power in sense amplifier circuits.

9 Hours

Unit V

Low energy computing using energy recovery techniques

Energy dissipation in transistor channel using an RC model, Energy recovery circuit design, Designs with partially reversible logic, Supply clock generation.

9 Hours

Unit VI[$]

Power and energy calculations for various VLSI circuits – measurement of glitches

Total: 45 Hours

Reference(s)

1. K.Roy and S.C. Prasad, *Low Power CMOS VLSI Circuit Design*, Wiley, 2000.
2. K.S. Yeo and K.Roy, *Low-Voltage, Low-Power VLSI Subsystems*, Tata McGraw-Hill, 2004.
3. Dimitrios Soudris, Chirstian Pignet and Costas Goutis, *Designing CMOS Circuits for Low Power*, Kluwer, 2009
4. James B. Kuo and Shin – Chia Lin, *Low voltage SOI CMOS VLSI Devices and Circuits*, John Wiley and Sons, 2001.
5. J.B Kuo and J.H Lou, *Low voltage CMOS VLSI Circuits*, Wiley, 1999.
6. Gary Yeap, *Practical Low Power Digital VLSI Design*, Kluwer, 1997.

15ES62 / 15AE69 PATTERN RECOGNITION AND ARTIFICIAL INTELLIGENT TECHNIQUES
(Common to Embedded Systems & Applied Electronics)

3 0 0 3

Course Objectives

- To understand different supervised and unsupervised learning techniques.
- To obtain sound knowledge on recent advancement on pattern recognition techniques.
- To gain knowledge about recent advances in neural networks and fuzzy logic.

Course Outcomes (COs)

The student will be able to

1. Formulate and describe various applications in pattern recognition.
2. Understand the Bayesian approach to pattern recognition and validate different clustering technique.
3. Understanding of the major areas and challenges of AI.

Unit I

Pattern Classifier

Overview of pattern recognition -Discriminant functions-Supervised learning –Parametric estimation-Maximum likelihood estimation –Bayesian parameter estimation- Perceptron algorithm-LMSE algorithm –Problems with Bayes approach –Pattern classification by distance functions-Minimum distance pattern classifier.

9 Hours

Unit II

Unsupervised Classification

Clustering for unsupervised learning and classification - Clustering concept-C-means algorithm-Hierarchical clustering procedures- Graph theoretic approach to pattern clustering - Validity of clustering solutions.

9 Hours

Unit III

Structural Pattern Recognition

Elements of formal grammars-String generation as pattern description - recognition of syntactic description-Parsing-Stochastic grammars and applications - Graph based structural representation.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit IV

Feature Extraction And Selection

Entropy minimization - Karhunen-Loeve transformation-feature selection through functions approximation-Binary feature selection.

9 Hours

Unit V

Recent Advances

Neural network structures for Pattern Recognition –Neural network based Pattern associators-Unsupervised learning in neural Pattern Recognition-Self organizing networks-Fuzzy logic-Fuzzy classifiers-Pattern classification using Genetic Algorithms.

9 Hours

Unit VI[$]

Density Estimation – Parzen Windows - KNN Estimation – The Nearest neighbor rule– Metrics and Nearest neighbor classification.

Total: 45 Hours

Reference(s)

1. R.O Duda, P.E Hart and Strok, *Pattern Classification*, Wiley, 2001.
2. Robert J. Sehalkoff, *Pattern Recognition: Statistical, Structural and Neural Approaches*, John Wiley & Sons Inc., 2007.
3. Tou Gonzales, *Pattern Recognition Principles*, Wesley Publication Company, 2000.
4. Morton Nadier and P. Eric Smith, *Pattern Recognition Engineering*, John Wiley & Sons, 2000.
5. *IEEE Transaction on Pattern Recognition Techniques*.
6. *IEEE Engineering Medicine and Biology Magazine*.

15ES63 DESIGN OF EMBEDDED CONTROL SYSTEMS

3 0 0 3

Course Objectives

- To expose the students to the fundamentals of Embedded System Blocks
- To teach the fundamental RTOS
- To discuss the Applications development using interfacing

Course Outcomes (COs)

The student will be able to

1. Compare types and Functionalities in commercial software tools.
2. Develop the Applications using interfacing.
3. Program for the process communication.

Unit I

Embedded System Organization

Embedded computing – characteristics of embedded computing applications – embedded system design challenges; Build process of Real time Embedded system – Selection of processor; Memory; I/O devices-Rs-485, MODEM, Bus Communication system using I2C, CAN, USB buses, 8 bit –ISA, EISA bus

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit II

Real-Time Operating System

Introduction to RTOS; RTOS- Inter Process communication, Interrupt driven Input and Output - Nonmaskable interrupt, Software interrupt; Thread – Single, Multithread concept; Multitasking Semaphores.

9 Hours

Unit III

Interface with Communication Protocol

Design methodologies and tools – design flows – designing hardware and software Interface . – system integration; SPI, High speed data acquisition and interface-SPI read/write protocol, RTC interfacing and programming

9 Hours

Unit IV

Design of Software for Embedded Control

Software abstraction using Mealy-Moore FSM controller, Layered software development, Basic concepts of developing device driver – SCI – Software - interfacing & porting using standard C & C++ ; Functional and performance Debugging with benchmarking Real-time system software – Survey on basics of contemporary RTOS – VXWorks, UC/OS-II

9 Hours

Unit V

Case Studies with Embedded Controller

Programmable interface with A/D & D/A interface; Digital voltmeter, control- Robot system; - PWM motor speed controller, serial communication interface.

9 Hours

Unit VI[$]

Fast Ethernet Controller bus- Micro C/OS-II RTOS -Embedded tool chain- Mixing C and Assembly- concurrent software - chocolate vending machine case study.

TOTAL : 45 Hours

Reference(s)

1. Steven F. Barrett, Daniel J. Pack, "Embedded Systems – Design and Applications with the 68HC 12 and HCS12", Pearson Education, 2008.
2. Raj Kamal, "Embedded Systems- Architecture, Programming and Design" Tata McGraw Hill, 2006.
3. Micheal Khevi, "The M68HC11 Microcontroller application in control, Instrumentation & Communication", PH NewJersy, 1997.
4. Chattopadhyay, "Embedded System Design",PHI Learning, 2011.
5. Muhammad Ali Mazidi, Rolin D. Mckinlay, Danny Causey, "PIC Microcontroller and Embedded Systems- Using Assembly and C for PIC18", Pearson Education,2008.
6. Steven F.Barrett,Daniel J.Pack, "Embedded Systems-Design & Application with the 68HC12 & HCS12", Pearson Education,2008.
7. Daniel W. Lewis, "Fundamentals of Embedded Software", Prentice Hall India, 2004.
8. Jack R Smith "Programming the PIC microcontroller with MBasic" Elsevier, 2007.
9. Keneth J.Ayala, "The 8086 Microprocessor: Programming & Interfacing the PC", Thomson India edition,

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES64 GRAPHICAL SYSTEM DESIGN

3 0 0 3

Course Objectives

- To learn the concepts towards measurement and automation with LabView.
- To get the knowledge about how to control an external measuring device by interfacing a computer.
- To become competent in data acquisition and instrument control.

Course Outcomes (COs)

The student will be able to

1. Build a virtual instrument using good coding practices.
2. Understand the programming structure used in system design.
3. Construct virtual instruments using LabVIEW, a visual system design software, for monitoring, analysing, and diagnosing physiological signals and imagery.

Unit I

Over view of Instrument

General Functional description of a digital instrument - Block diagram of a Virtual Instrument - Physical quantities and Analog interfaces - Hardware and Software - User interfaces - Advantages of Virtual instruments over conventional instruments - Architecture of a Virtual instrument and its relation to the operating system

9 Hours

Unit II

Common Instrument Interfaces

Current loop, Interface buses: USB, PCMCIA, VXI, SCXI, and PXI. Networking Basics for Industrial automation. Instrumentation Bus- HART,RS232, RS422, RS485, IEC/ISA Field Bus, ZigBee, Bluetooth.

9 Hours

Unit III

Programming Structure

FOR loops, WHILE loop, CASE structure, formula node, Sequence structures - Arrays and Clusters - Array operations - Bundle - Bundle/Unbundle by name, graphs and charts - String and file I/O - High level and Low level file I/Os - Attribute modes Local and Global variables.

9 Hours

Unit IV

Hardware Aspects

Installing hardware, installing drivers - Configuring the hardware - Addressing the hardware in LabVIEW - Digital and Analog I/O function - Data Acquisition - Buffered I/O - Real time Data Acquisition.

9 Hours

Unit V

Graphical system Design Software Language Labview Applications

Motion Control: General Applications - Feedback devices, Motor Drives – Machine vision – LabVIEW IMAQ vision – Machine vision Techniques – Configuration of IMAQ DAQ Card - Instrument Connectivity.

9 Hours

Unit VI[$]

GPIB, IEEE 488, IEEE 488.2,HS488, Serial Communication - General, GPIB Hardware & Software specifications - PX1 / PC1: Controller and Chassis Configuration

Total: 45 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Reference(s)

1. Jerome Jovitha, Virtual Instrumentation Using Labview, PHI Learning Pvt. Ltd., 2012
2. S Gupta and J P Gupta, PC Interfacing for Data Acquisition and Process Control, Second Edition, Instrument Society of America, Reprint 1995.
3. Krishna Kant, Computer Based Industrial Control, Prentice Hall India Ltd., 2004.
4. Bouwens, A.J., Digital Instrumentation, McGraw Hill, Reprint 2007.
5. Garry W Johnson, LabView Graphical Programming, Tata McGraw Hill, 3rd Edition, 2001.
6. Sanjay Gupta and Joseph John, Virtual Instrumentation Using LabVIEW, Tata McGraw-Hill, Ist edition, 2008.
7. Reference Tutorials and application Notes for National Instruments sites www.ni.com/academic.

15ES65 / 15VL51 ASIC DESIGN
(Common to Embedded Systems & VLSI Design)

3 0 0 3

Course Objectives

- To acquire knowledge about different types of ASICs design.
- To study about various types of Programmable ASICs architectures and interconnects.
- To comprehend the low power design techniques and methodologies.

Course Outcomes (COs)

The student will be able to

1. Analysis the different types of ASICs design.
2. Analysis the different Logic cell architecture and interconnects.
3. Analysis about different programmable ASIC design software.

Unit I

Introduction to ASICS, CMOS Logic, ASIC Library Design

Types of ASICs - Design flow – CMOS transistors- CMOS Design rules –Combinational logic Cell Sequential logic cell - Transistor as Resistors - Transistor parasitic capacitance – Logical effort - Library cell design – Library architecture- gate array design- standard cell design-data path cell design.

9 Hours

Unit II

Programmable ASICS, Programmable ASIC Logic Cells and Programmable ASIC I/O Cells

Anti fuse - Static RAM - EPROM and EEPROM technology - PREP benchmarks - Actel ACT - Xilinx LCA –Altera FLEX - Altera MAX- DC & AC inputs and outputs – clock input-power input - Xilinx I/O blocks.

9 Hours

Unit III

Programmable ASIC Interconnect, Programmable ASIC Design Software and Low Level Design Entry

Actel ACT -Xilinx LCA - Xilinx EPLD - Altera MAX 5000 and 7000 - Altera MAX 9000 - Altera FLEX –Design systems - Logic Synthesis - Half gate ASIC -Low level design language - PLA tools EDIF- CFI design representation.

9 Hours

Unit IV

ASIC construction

Physical design- CAD tools- system partitioning- estimating ASIC size- power dissipation- FPGA partitioning- partitioning methods.

9 Hours

Unit V

Floorplanning, Placement and Routing

Floorplanning –placment- physical design flow- information formats- Routing- Global routing, detailed routing, special routing, circuit extraction and DRC.

9 Hours

Unit VI[$]

ASIC implementation of basic VLSI combinational and sequential circuits

Total: 45 Hours

Reference(s)

1. M.J.S. Smith, *Application Specific Integrated Circuits*, Pearson Education, 2008.
2. Farzad Nekoogar and Faranak Nekoogar, *From ASICs to SOCs: A Practical Approach*, Prentice Hall PTR, 2003.
3. Wayne Wolf, *FPGA-Based System Design*, Prentice Hall PTR, 2009.
4. R.Rajsuman, *System-on-a-Chip Design and Test*, Santa Clara, CA: Artech House Publishers, 2000.
5. F.Nekoogar, *Timing Verification of Application-Specific Integrated Circuits (ASICs)*, Prentice Hall PTR, 1999.
6. S.Srinivasan, *VLSI Circuits*, NPTEL Courseware, 2007.

15ES66 WIRELESS AND MOBILE COMMUNICATION

3 0 0 3

Course Objectives

- To understand the Cellular Mobile Networks
- To provide a comprehensive background knowledge of Wireless Communication
- To study the various broadband technologies

Course Outcomes (COs)

The student will be able to

1. Demonstrate knowledge of protocols used in wireless communications.
2. Understand the cellular radio concepts such as frequency reuse, handoff and how interference between mobiles and base stations affects the capacity of cellular systems.
3. Describe current and future cellular mobile communication systems (GSM, IS95, WCDMA, etc).

Unit I

Overview of Networks

Wireless Transmission- signal propagation-spread spectrum-Satellite Networks - Capacity Allocation-FAMA-DAMA-MAC

9 Hours

Unit II

Mobile Networks

Cellular Wireless Networks – GSM – Architecture – Protocols – Connection Establishment - Frequently Allocation-Routing – Handover – Security - GPRA

9 Hours

Unit III

Wireless Networks

WirelessLAN-IEEE802.11Standard-Architecture-Services – AdHocNetwork – HiperLAN - Bluetooth

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit IV

Routing

Mobile IP-DHCP- AdHoc Networks - Proactive and Reactive Routing Protocols - Multicast Routing

9 Hours

Unit V

Transport and Application Layers

TCP over AdhocNetworks – WAP – Architecture – WWW Programming Model – WDPWTLS – WTP – WSP – WAE –WTA Architecture – WML – WML scripts.

9 Hours

Unit VI[$]

ISA/PCI Bus protocols - Data Centric routing - Network Topology - Energy efficient and robust routing - WML

Total: 45 Hours

Reference(s)

1. KavehPahlavan, Prasanth Krishnamoorthy, *Principles of Wireless Networks*, PHI/Pearson Education, 2003
2. UweHansmann, LotharMerk, Martin S.Nicklons and Thomas Stober, *Principles of Mobile computing*, Springer, Newyork, 2003.
3. C.K.Toh, *AdHoc mobile wireless networks*, Prentice Hall Inc, 2002.
4. Charles E.Perkins, *Adhoc Networking*, Addison-Wesley, 2001.
5. Jochen Schiller, *Mobile communications*, PHI/Pearson Education, Second Edition, 2003.
6. William Stallings, *Wireless communications and Networks*, PHI/Pearson Education, 2002.

15ES67 DISTRIBUTED EMBEDDED COMPUTING

3 0 0 3

Course Objectives

- To understand the hardware infrastructure of distributed systems.
- To study concepts of Internet and Embedded agent.
- To obtain basic knowledge distributed computing using Java.

Course Outcomes (COs)

The student will be able to

1. Understand network protocol layers and explain the specific role of each.
2. Understand complete design of an embedded system with functional requirements for hardware and software components
3. Develop software systems for measurement of embedded system operating characteristics (for example, latency, data transport rate, error rate).

Unit I

The Hardware Infrastructure

Broad Band Transmission facilities, Open Interconnection standards, Local Area Networks, Wide Area Networks, Network management, Network Security, Cluster computers.

9 Hours

Unit II

Internet Concepts

Capabilities and limitations of the internet, Interfacing Internet server applications to corporate databases HTML and XML Web page design and the use of active components.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit III

Distributed Computing using Java

I/O streaming, Object serialization, Networking, Threading, RMI, multicasting, distributed databases, embedded java concepts, case studies.

9 Hours

Unit IV

Embedded Agent

Introduction to the embedded agents, Embedded agent design criteria, Behaviour based, Functionality based embedded agents, Agent co-ordination mechanisms and benchmarks embedded agent, Case study: Mobile robots.

9 Hours

Unit V

Embedded Computing Architecture

Synthesis of the information technologies of distributed embedded systems, analog/digital co-design, optimizing functional distribution in complex system design, validation and fast prototyping of multiprocessor system-on-chip, dynamic scheduling algorithm for real-time multiprocessor systems.

9 Hours

Unit VI[$]

Embedded computing architecture and validation, fast prototyping of multiprocessor system-on-chip, dynamic scheduling algorithm for real-time multiprocessor systems.

Total: 45 Hours

Reference(s)

1. Dietel and Dietel, *JAVA how to program*, Prentice Hall, 2004.
2. George Coulouris and Jean Dollimore, Distributed *Systems – concepts and design*, Addison Wesley, 2002.
3. Bernd Kleinjohann, *Architecture and Design of Distributed Embedded Systems*, Kluwer Academic Publishers, 2001.
4. *www.embedded-journal.org*
5. *www.embeddedtechnologyjournal.com*

15ES68 FAULT TOLERANCE COMPUTING

3 0 0 3

Course Objectives

- To study about the fundamentals of molding.
- To understand detection and simulation faults.
- To gain sound knowledge about various testing techniques.

Course Outcomes (COs)

The student will be able to

1. Understand the Software testing and fault tolerant systems
2. Perform Information redundancy using some types of error detecting/correcting codes
3. Analyze a system for performance-dependability tradeoffs.

Unit I

Modeling

Basic Concept, Functional modeling at the logic level, Functional models at the register level, Structural models, Level of modeling. Type of simulation, unknown logic value, compiled simulation, Event-driven simulation and Hazard Detection.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit II

Fault Detection

Logical fault models, Fault detection and redundancy, Fault equivalence and fault location, Fault Dominance, Single stuck-fault models, multiple stuck fault model, stuck RTL variables, Fault variables.

9 Hours

Unit III

Simulation

Testing for Single Stuck fault and Bridging fault. General fault simulation techniques, Serial Fault simulation, Parallel fault simulation, Deductive fault simulation, Concurrent fault simulation, Fault simulation for combinational circuits, Fault sampling, Statistical fault analysis.

9 Hours

Unit IV

Checking

General aspects of compression techniques, ones- count compression, transition – count compression, Parity – check compression, Syndrome testing and Signature Analysis Basic concepts , Multiple – Bit Errors , Checking circuits and self-checking , self– checking checkers , Parity – check function , totally self-checking m/n code checkers , totally self-checking equality checkers , Self-checking Berger code checkers and self-checking combinational circuits.

9 Hours

Unit V

Testing

Built In Self-Test, Self-testing circuits for systems, memory & processor testing, PLA testing, Automatic test pattern generation and Boundary Scan Testing - JTAG

9 Hours

Unit VI[$]

Level of modeling - Fault variables - Fault sampling - POST - Encryption and decryption of checking.

Total: 45 Hours

Reference(s)

1. M.Abramovici, M.A. Breuer, A.D. Friedman, *Digital systems testing and testable design*, Jaico Publishing House, 2001.
2. Diraj K. Pradhan, *Fault Tolerant Computer System Design*, Prentice Hall, 1996.
3. Dubrova, Elena, *Fault-Tolerant Design*, springer, 2013.

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ES69 ANALOG INTERFACING

3 0 0 3

Course Objectives

- To Understand the large and small signals and use MOS transistor models and to identify three basic amplifier configurations.
- To Use two-stage amplifier configurations and understand the differential pair and its offsets and common-mode rejection.
- To Perform DC and AC analysis of the standard operational amplifier and understand high performance operational amplifier design for low offset, low input current and low offset drift

Course Outcomes (COs)

The student will be able to

1. Understand analog circuit behavior in both linear and nonlinear operation.
2. Parse large circuits and systems into smaller, analyzable subunits, analyze them, and then apply the understanding gained from that process to analyze the system as a whole, including for noise and variation.
3. Implement a circuit or subsystem at the transistor level to solve an open-ended problem and effectively communicate the constraints and critical aspects of that system.

Unit I

MOSFETs

Device Structure and Physical Operation - Current-Voltage Characteristics - MOSFET Circuits at DC - The MOSFET as an Amplifier and as a Switch - Biasing in MOS Amplifier Circuits - Small-Signal Operation and Models - Single-Stage MOS Amplifiers – High-Frequency Response

9 Hours

Unit II

Single-Stage Integrated-Circuit Amplifiers

IC Design Philosophy - Comparison of the MOSFET and the BJT - IC Biasing—Current Sources, Current Mirrors, and Current Steering Circuits - High-Frequency Response – CS, CG, CD amplifier with active loads, cascade amplifier

9 Hours

Unit III

Differential and Multistage Amplifiers

The MOS Differential Pair - Small-Signal Operation of the MOS Differential Pair - Other Non ideal Characteristics of the Differential Amplifier - The Differential Amplifier with Active Load - Frequency Response of the Differential Amplifier - Multistage Amplifiers

9 Hours

Unit IV

Feedback circuits

The General Feedback Structure - Properties of Negative Feedback - Four Basic Feedback Topologies - Series-Shunt Feedback Amplifier - Series-Series Feedback Amplifier - The Shunt-Shunt and Shunt-Series Feedback Amplifiers - Determining the Loop Gain - The Stability Problem - Effect of Feedback on the Amplifier Poles - Stability Study Using Bode Plots - Frequency Compensation

9 Hours

Unit V

Operational-Amplifier

Op-Amp Circuit - DC Analysis of the 741 - Small-Signal Analysis of the 741 - Gain, Frequency Response, and Slew Rate of the 741 - Op Amp Noise Theory and Applications - Understanding Op Amp Parameters - Instrumentation: Sensors to A/D Converters - Designing Low-Voltage Op Amp Circuits

9 Hours

Unit VI[$]

High-Frequency Response of MOSFET - The Stability Problem - Effect of Feedback on the Amplifier Poles - Stability Study Using Bode Plots - Frequency Compensation - Determining the Loop Gain - Understanding Op Amp Parameters.

Total: 45 +15 Hours

Reference(s)

1. Adel S Sedra and Kenneth C Smith, *Micro Electronic circuits*, Oxford University Press, 2004.
2. Ron Mancini , *OP Amps for everyone*, Texas Instruments, An imprint of Elsevier 2005
3. *Meeting signal Path Design Challenges,* by National Semiconductors Analog University of National Semiconductors

15ES70 OPERATING SYSTEMS

3 0 0 3

Course Objectives

- To describe the general architecture of computers
- To describe, contrast and compare differing structures for operating systems
- To understand and analyse theory and implementation of processes, Scheduling, Tasks and Memory

Course Outcomes (COs)

The student will be able to

1. Understand the types of operating systems and differences among them.
2. Understand the structure and design decisions involved in the implementation of an operating system.
3. Understand Files and storage of persistent information, types of files and file access.

Unit I

Operating System Overview

Computer system: Evolution of the Microprocessor - Instruction Execution – Interrupts - The Memory Hierarchy - Cache Memory - Direct Memory Access - Multiprocessor and Multicore Organization, Operating System: The Evolution of Operating Systems, Developments Leading to Modern Operating Systems, Virtual Machines, OS Design Considerations for Multiprocessor and Multicore Processor.

9 Hours

Unit II

Process Management

Processes: Process Concept, Process Scheduling, Operations on Processes, Inter-process Communication, Threads: Multithreading Models, Thread Libraries, Threading Issues. Scheduling: Types of Processor Scheduling - Scheduling Algorithms - Multiprocessor Scheduling - Real-Time Scheduling, Process Synchronization, Deadlocks.

9 Hours

Unit III

Memory Management

Main Memory: Memory Management Requirements - Memory Partitioning - Contiguous Memory Allocation - Paging - Segmentation, - Security Issues, Virtual Memory: Demand Paging - Copy-on-Write - Page Replacement - Allocation of Frames – Thrashing - Memory-Mapped Files - Allocating Kernel Memory

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit IV

Input/Output and File Management

I/O Devices: Organization of the I/O Function - I/O Buffering - Disk Scheduling – RAID - Disk Cache, File system: File Organization and Access - B-Trees - File Directories - File Sharing - Record Blocking - Secondary Storage Management - File System Security

9 Hours

Unit V

Embedded Operating Systems and Distributed Systems

Characteristics of Embedded Operating Systems – eCos – TinyOS, Client/Server Computing - Service-Oriented Architecture - Distributed Message Passing - Remote Procedure Calls - Clusters

9 Hours

Unit VI[$]

configurable processors and multi-core processors - Scratch Pad Memory (SPM) - Memory management and system initialization - Input and Output in S12X processor - Embedded Operating Systems OS-less system.

Total: 45 Hours

References

1. William Stallings, *Operating systems: Internals and design Principles*, Prentice Hall, Sixth edition, 2009.
2. Abraham Sibershatz, Peter Baer galvin and Creg Gagne, *Operating Systems Concepts*, Sixth edition , John wiley & sons , 2004.
3. Gary Nut, Nabendu and Sarmistha Neogy, *Operating systems*, Pearson Education, 2009

15ES71 / 15VL64 NETWORK ON CHIP
(Common to Embedded Systems & VLSI Design)

3 0 0 3

Course Objectives

- To understand the fundamentals of 3D NOC.
- To impart knowledge about testing and energy issues in NOC.
- To understand the router architectures in 3D NOC.

Course Outcomes (COs)

The student will be able to

1. Understand the need for 3D NOC.
2. Know the concepts used in testing and reduction of power in NOC.
3. Learn the architecture and working of routers in 3D NOC.

Unit I

Introduction to Three Dimensional NOC

Three-Dimensional Networks - on-Chips Architectures - Resource Allocation for QoS On-Chip Communication - Networks-on-Chip Protocols-On-Chip - Processor Traffic Modeling for Networks-on-Chip.

9 Hours

Unit II

Test and Fault Tolerance of NOC

Design-Security in Networks-on-Chips-Formal Verification of Communications in Networks-on-Chips-Test and Fault Tolerance for Networks-on-Chip Infrastructures- Monitoring Services for Networks-on-Chips.

9 Hours

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

Unit III

Energy and Power Issues of NOC

Energy and Power Issues in Networks-on-Chips-The CHAIN works Tool Suite: A Complete Industrial Design Flow for Networks-on-Chips

9 Hours

Unit IV

Micro-Architecture of NOC Router

Baseline NoC Architecture – MICRO-Architecture Exploration ViChaR: A Dynamic Virtual Channel Regulator for NoC Routers- RoCo: The Row-Column Decoupled Router – A Gracefully Degrading and Energy-Efficient Modular Router Architecture for On-Chip Networks. Exploring Fault Tolerant Networks-on-Chip Architectures.

9 Hours

Unit V

DimDE Router for 3D NOC

A Novel Dimensionally-Decomposed Router for On-Chip Communication in 3D Architectures-Digest of Additional NoC MACRO-Architectural Research.

9 Hours

Unit VI[$]

ViChaR router – Wormhole router – RoCo Row Column Decoder router.

Total: 45 Hours

Reference(s)

1. Chrysostomos Nicopoulos, Vijaykrishnan Narayanan, Chita R.Das, *Networks-on- Chip Architectures AHolistic Design Exploration,* Springer, 2009.
2. Fayezgebali, Haythamelmiligi, Hqhahed Watheq E1-Kharashi, *Networks-on-Chips theory and practice,* CRC press, 2009.
3. Axel Jantsch , Hannu Tenhunen, *Networkson Chip*, Publisher: Springer; Soft cover reprint of hardcover 1st ed. 2003 edition (November 5, 2010).
4. Giovanni De Micheli , Luca Benini, *Networkson Chips: Technology and Tools (Systems on Silicon)*, Publisher: Morgan Kaufmann; 1 edition (August 3, 2006).
5. Jose Flich , DavideBertozzi, *Designing Network On-Chip Architectures in the Nanoscale Era*, Publisher: Chapman and Hall/CRC; 1 edition (December 18,2010)

[$] Includes Self Study topics of all 5 units and considered for Continuous Assessment only.

15ESXA Quad Core

1 0 0 1

Course Objectives

- To understand the fundamentals of Quad core processors/controllers.
- To gain knowledge in assembly language programming to perform basic input/output and interface with external devices using micro-controllers.

Course Outcomes (COs)

Students will be able to

1. Discuss the modern architectural concepts
2. Identify the correct processor for a given task
3. Employ assembly language programming
4. Design hardware and software system implementations using micro-controllers

Architecture of the AMD Core - Functional Units - Cache Architecture - Memory interface - Using Cray Linux Environment (CLE)- Modules - Setting up and submitting a parallel job - CLE I/O details - Compiler considerations when using the Dual Core - Memory pre-fetching - How to use shared memory parallelization in the compiler - Optimizations for the AMD Dual Core - Optimization techniques that the application developer needs to know - Blocking for cache - Using prefetch directives - Quad core considerations - I/O Optimization on Lustre - Using Craypat to examine hardware counters for understanding cache utilization and vectorization - Using Apprentice2 - Optimizing for the Distributed Shared Memory MPP - Optimization techniques that application developer need to know about - MPI - OpenMP - Pthreads- Mixing MPI and OpenMP/Pthreads - Math Libraries - Using Apprentice to examine MPI performance.COM Express Modules with Quad-Core Third Generation Core Processors - IBM System p5 Quad-Core Module Based on POWER5+ Technology - i.MX 6 Series Applications Processors.

Total: 20 hours

15ESXB Arduino

1 0 0 1

Course Objectives

- To Study the Arduino platform, language and programming environment and the Processing programming language as used to communicate with Arduino.
- To Learn how to develop practical interaction-rich applications consisting of computer systems and sensors using Arduino and Processing.
- To understand the basic principles of networks with emphasis on issues relevant to complex media applications.

Course Outcomes (COs)

Students will be able to

1. Explain the relationship between computer hardware and software.
2. Understand how sensors integrate into computer systems through hardware and application development environment .
3. Develop interactive applications involving the computer system communicating with sensors, Arduino and the Processing language.

Getting Started - Exploring the Arduino Board and the IDE - First Steps - Building Blocks - Working with Functions - Numbers, Variables, and Arithmetic - Liquid Crystal Displays - Expanding Your Arduino - Numeric Keypads - Accepting User Input with Touchscreens - Meet the Arduino Family - Motors and Movement - Using GPS with Your Arduino - Wireless Data - Infrared Remote Control - Reading RFID Tags - Data Buses - Real-time Clocks - The Internet - Cellular Communications.

Total: 20 Hours

15ESXC ATMEL

1 0 0 1

Course Objectives

- To understand the basics of ATMEL.
- To acquire Knowledge in programming and application development using microcontroller.
- To understand the memory structure of Atmel controller.

Course Outcomes (COs)

- Understand the purpose of atmel studio 6.
- Develop a real time design product using Atmega128.

Introduction - Purpose - Atmel Studio 6 Overview - ATmega128Overview – Nomenclature – Disclaimer - AtmelStudio6 4 : Startup Tutorial - Installation - Project Creation - Project Simulation - Simulation Tips - Line-By-Line Debugging - Workspace Window - Memory Windows - Debugging Strategies - Programming the ATmega128 : Parts and Cables Needed - Downloading the Necessary Software - Connecting the Universal Programmer - Programming Your Microcontroller. ATmega128 : Useful Registers - General Purpose Registers - Special Function Registers - Interrupt Vectors - Memory Specifications - Program Memory - SRAM Data Memory - EEPROM Data Memory - Starter Code - Code style - Design style - Directory structure.

Total: 20 hours